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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,534	12/08/2003	William Voorhees	LSI.84US01 (03-0055)	4544
24319	7590	12/05/2005	EXAMINER	
LSI LOGIC CORPORATION 1621 BARBER LANE MS: D-106 MILPITAS, CA 95035			HOLLINGTON, JERMELE M	
			ART UNIT	PAPER NUMBER
			2829	

DATE MAILED: 12/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/731,534

Applicant(s)

VOORHEES ET AL.

Examiner

Jermele M. Hollington

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 08 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 3-10, 12-19 and 21-26 is/are rejected.
- 7) ☒ Claim(s) 2, 11 and 20 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-10, 12-19 and 21-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Verdun (5805833).

Regarding claims 1, 10 and 19, Verdun discloses [see Fig. 3] a switchable probe board (unit interface 150) for probing a parallel bus (bus 165) comprising: a connector (connector 65) adapted to connect into said parallel bus (165); a plurality of signal paths (pin connectors 255) corresponding to individual signals of said parallel bus (165), each of said plurality of signal paths (255) having a passive filter, and an adjustable filter circuit, said plurality of signal paths (255) being electrically communicated to said connector (65); a switch matrix (I/O port 85) connected to each of said plurality of signal paths (255) and having at least one output; and a controller (computer system 15) adapted to configure said switch matrix (85) to connect one of said plurality of signal paths (255) to said at least one output, said controller (15) having an input; wherein said switchable probe board (150) is a single printed circuit board.

Regarding claims 3, 12 and 21, Verdun discloses said controller (15) comprises a microprocessor (processor 180) programmable to cause said switch matrix (85) to sequentially switch a predetermined set of said plurality of signal paths (255) to said at least one output.

Regarding claims 4, 13 and 22, Verdun discloses said controller (15) is adapted to communicate on a second communications bus (165).

Regarding claims 5, 14 and 23, Verdun discloses said controller (15) is adapted to be programmed by a second device communicating (PCI bridge 195) over said second communications bus (165).

Regarding claims 6, 15 and 24, Verdun discloses said adjustable filter circuit [via signal path 255] is adapted to receive a training pattern of signals on said parallel bus (165) and setting said adjustable filter circuit to a skew value based on said training pattern.

Regarding claims 7-8, 16-17 and 25-26, Verdun discloses said parallel bus is a PCI or SCSI bus.

Regarding claims 9, 18 and 27, Verdun discloses mounting hardware (expansion side 160) adapted to simulate the mounting hardware of a disk drive.

### ***Conclusion***

The examiner will like to note in claims 1, 4-6, 9-10, 13-15, 18, 22-24 and 26 the limitation "adapted to" is not considered as a positive limitation since it has been held that the recitation that an element is "adapted to" perform only requires the ability to so perform and it does not limit a claim to a particular structure and it does not limit the scope of a claim or claim limitation.

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. McCombs (5778194), Cepulis et al (6061754), Klein (6311245), Richmond et al (6562636, 6682945) and Reed et al (6832339) disclose a method and apparatus for measuring a performance of a particular bus.

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4. Claims 2, 11 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

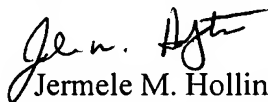
5. The following is a statement of reasons for the indication of allowable subject matter: regarding claims 2, 11 and 20, the reason for the allowance of the claims is due to a switchable probe board comprising a controller comprises dip switches.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (517) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMH  
December 1, 2005

  
Jermele M. Hollington  
Primary Examiner  
Art Unit 2829